

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently amended) A thin film transistor array panel comprising:
an insulating substrate;
a plurality of gate lines formed on the insulating substrate;
a plurality of storage electrode lines formed on the first insulating substrate and including a storage electrode;
a plurality of data lines insulated from the gate lines and intersecting the gate lines; and
a plurality of group pixel areas arranged in a matrix, each group one of the pixel areas comprising:
a first electrode and a second electrode disposed on the pixel area;
a third electrode connected to the first pixel electrode and overlapping at least one of the first electrode and the second electrode;
~~a pair of first and second pixel electrodes capacitively coupled to each other, disposed on pixel areas defined by intersections of the gate lines and the data lines and arranged in a matrix;~~
~~a first thin film transistor connected to one of the gate lines and one of the data lines, and connected to the first pixel electrode; and~~
a second thin film transistor connected to or capacitively coupled to the second pixel electrode; and
~~a coupling electrode connected to one of the first pixel electrode and the second pixel electrode and overlapping the other of first pixel electrode and the second pixel electrode;~~
wherein a portion of the third electrode extends parallel to one of the data lines and the coupling electrode partially overlaps the storage electrode line.

2. (Currently Amended) The thin film transistor array panel of claim 1, wherein the storage electrode line and the coupling electrode overlaps an edge of one of the first electrode and the second pixel electrode[[s]].

3. (Currently Amended) The thin film transistor array panel of claim 2, wherein the coupling third electrode is connected to a drain electrode of ~~one of the first thin film transistor and the second thin film transistor.~~

4. (Previously Presented) The thin film transistor array panel of claim 3, wherein the second thin film transistor is connected to one of the storage electrode lines and the data lines.

5. (Currently Amended) The thin film transistor array panel of claim 4, wherein the second thin film transistor is connected to one of the storage electrode lines, and ~~each group~~ one of the pixel areas further comprises a third thin film transistor connected to one of the data lines, the second pixel-electrode, and one of the gate lines connected to the second thin film transistor.

6. (Currently Amended) The thin film transistor array panel of claim 1, wherein at least one of the first pixel-electrode and the second pixel-electrode comprises at least one domain partitioning member.

7. (Currently Amended) The thin film transistor array panel of claim 2, further comprising:

a gate insulating layer disposed between the gate lines and the data lines; and

a passivation layer disposed between the data lines and the first and the second pixel electrodes,

wherein the ~~coupling~~ third electrode is connected to the first pixel-electrode through a ~~contact~~ contact hole at the passivation layer.

8. (Currently Amended) A liquid crystal display comprising:

a first insulating substrate;

a gate line formed on the first insulating substrate and including first and second gate electrodes;

a storage electrode line formed on the first insulating substrate;

a gate insulating layer covering the gate line and the storage electrode line;

first and second amorphous silicon layers formed on the gate insulating layer;

a data line formed on the gate insulating layer and including a first source electrode disposed on the first amorphous silicon layer at least in part;

a second source electrode disposed on the second amorphous silicon layer at least in part;

[[]]first and second drain electrodes formed on the first and the second amorphous silicon layers at least in part and disposed opposite the first and the second source electrodes, respectively;

a coupling electrode formed on the gate insulating layer;

a passivation layer formed on the data line, the first and the second drain electrodes, and

the coupling electrode;

a first pixel electrode that is formed on the passivation layer and is connected to or overlaps the first drain electrode and the coupling electrode;

a second pixel electrode insulating from the first pixel electrode, connected to or overlaps the first drain electrode and the coupling electrode;

a second insulating layer facing the first insulating substrate; and

a common electrode formed on the second insulating substrate,

wherein a portion of the coupling electrode extends parallel to one of the data lines and partially overlaps the storage electrode line.

9. (Original) The liquid crystal display of claim 8, wherein the second source electrode is connected to the storage electrode line or the data line.

10. (Original) The liquid crystal display of claim 9, wherein the second source electrode is connected to the storage electrode line, and the liquid crystal display further comprises a third gate electrode connected to the gate line, a third source electrode connected to the data line, and the third drain electrode connected to the second pixel electrode.

11. (Original) The liquid crystal display of claim 9 or 10, wherein the first drain electrode is connected to the coupling electrode.

12. (Previously Presented) The liquid crystal display of claim 10, wherein the coupling electrode is connected to the first pixel electrode through a contact hole at the passivation layer.

13. (Currently Amended) The liquid crystal display of claim 12, further comprising:
~~a first domain partitioning member disposed on at least one of the first and the second substrates; and~~

a first domain partitioning member disposed on at least one of the first and the second substrates and partitioning a pixel area into a plurality of domains along with the first domain partitioning member.

14. (Previously Presented) The thin film transistor array panel of claim 1, wherein two storage lines of the plurality of storage electrode lines disposed opposite each other with respect to one gate line of the plurality of gate lines are connected to each other through a storage bridge.